AMENDMENTS TO THE SPECIFICATION:

Page 9; please insert the following paragraph after paragraph 0019:

FIGURE 4 illustrates a block diagram of an embodiment of a sleep mode voltage controller constructed according to the principles of the present invention.

Page 16; please replace paragraphs 0030 and 0031 with the following amended paragraphs:

In some embodiments, the sleep mode voltage controller 140 may provide the array high supply voltage V_{ADD}, the array low supply voltage V_{ASS} and the well voltage at optimum values for a set of transistor parameters. For example, the sleep mode voltage controller 140 may provide the array high supply voltage V_{ADD} at about 0.8 volts, the array low supply voltage V_{ASS} at about 0.4 volts and the n-well voltage V_{nwell} at about 1.2 volts for a general technology class of transistors. Thus, the SRAM array may have about 0.4 volts back bias on both the n-channel and the p-channel in addition to about 0.4 volts across the SRAM cell, as shown in FIGURE 4.

Additionally, the sleep mode voltage controller 140 may provide an adjustable array high supply voltage V_{ADD} and array low supply voltage V_{ASS}. Thus, the sleep mode voltage controller 140 may allow fine tuning of SRAM array 110 voltages for the sleep mode to obtain optimum values to reduce current leakage. The sleep mode

voltage controller 140 may adjust the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} based on a process corner transistor parameter. For example, for a strong-n/weak-p corner, V_{ADD} and V_{ASS} may be made higher than for a weak-n/strong-p corner so as to apply more back bias to the n-channel transistors. Conversely, for a weak-n/strong-p corner, V_{ADD} and V_{ASS} may be made relatively lower to apply more back bias to the p-channel transistors. Similarly, a relatively higher V_{ADD} and relatively lower V_{ASS} may be applied for a weak-n/weak-p corner relative to a strong-n/strong-p corner to optimize the trade-off of diode current and subthreshold current.

Pages 20-21, please replace paragraph 0040 with the following amended paragraph:

After employing the SRAM array, both an array high supply voltage V_{ADD} that is lower than a high operating voltage V_{DD} and an array low supply voltage V_{ASS} that is higher than a low operating voltage V_{SS} are provided to the SRAM array during a sleep mode in a step 320. In one embodiment, the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} may be provided based on transistor parameters of the SRAM array. The array high supply voltage V_{ADD} may be provided relative to a well voltage, such as, an n-well voltage. The array low supply voltage V_{ASS} may be provided relative a substrate voltage.